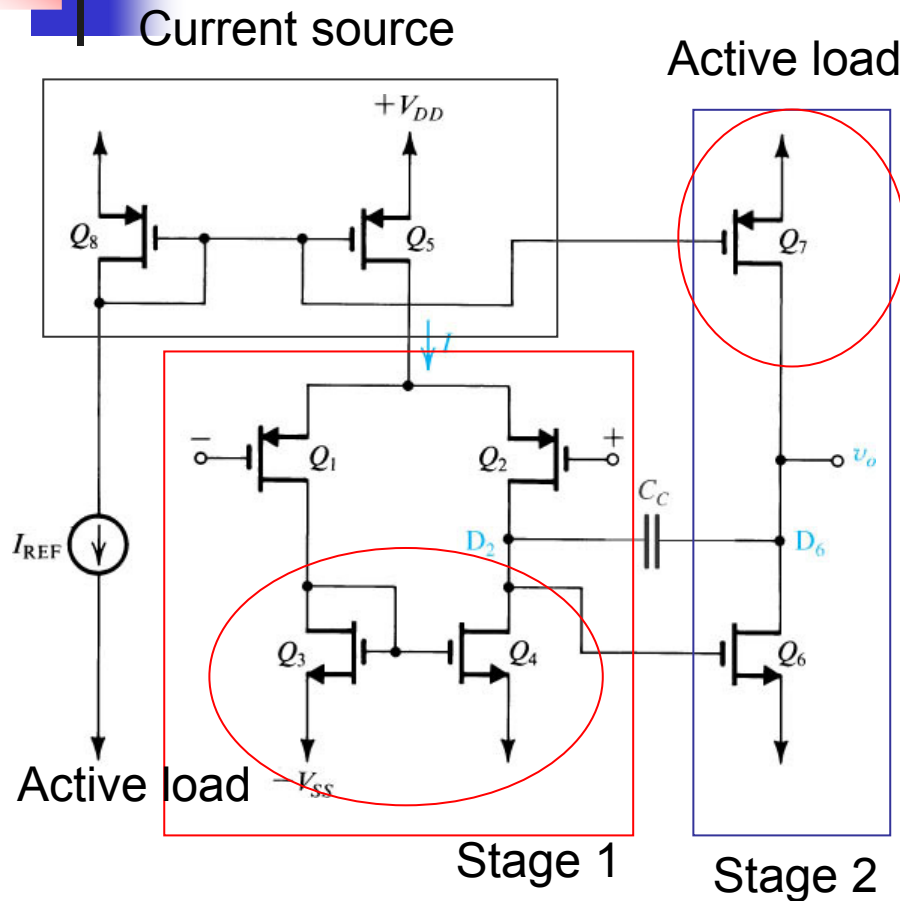




전자 회로 2

Lecture 9 (Multi-stage Amp.)

A two-stage CMOS Op Amp.



Design for minimizing systematic offset voltage:

Q1/Q2, Q3/Q4: perfect matching
+voltage = - voltage

$$\rightarrow V_{D3} = V_{D4} = -V_{SS} + V_{GS4}$$

$$\rightarrow V_{G6} = V_{D4} \rightarrow V_{GS6} = V_{GS4}$$

$$\rightarrow I_6 = I_7 \cdot (W/L)_6 / (W/L)_4$$

$$I_7 = I \cdot (W/L)_7 / (W/L)_5$$

$$\rightarrow I_6 = I_7 \text{ 이 되려면}$$

$$\rightarrow (W/L)_6 / (W/L)_4 = 2(W/L)_7 / (W/L)_5$$

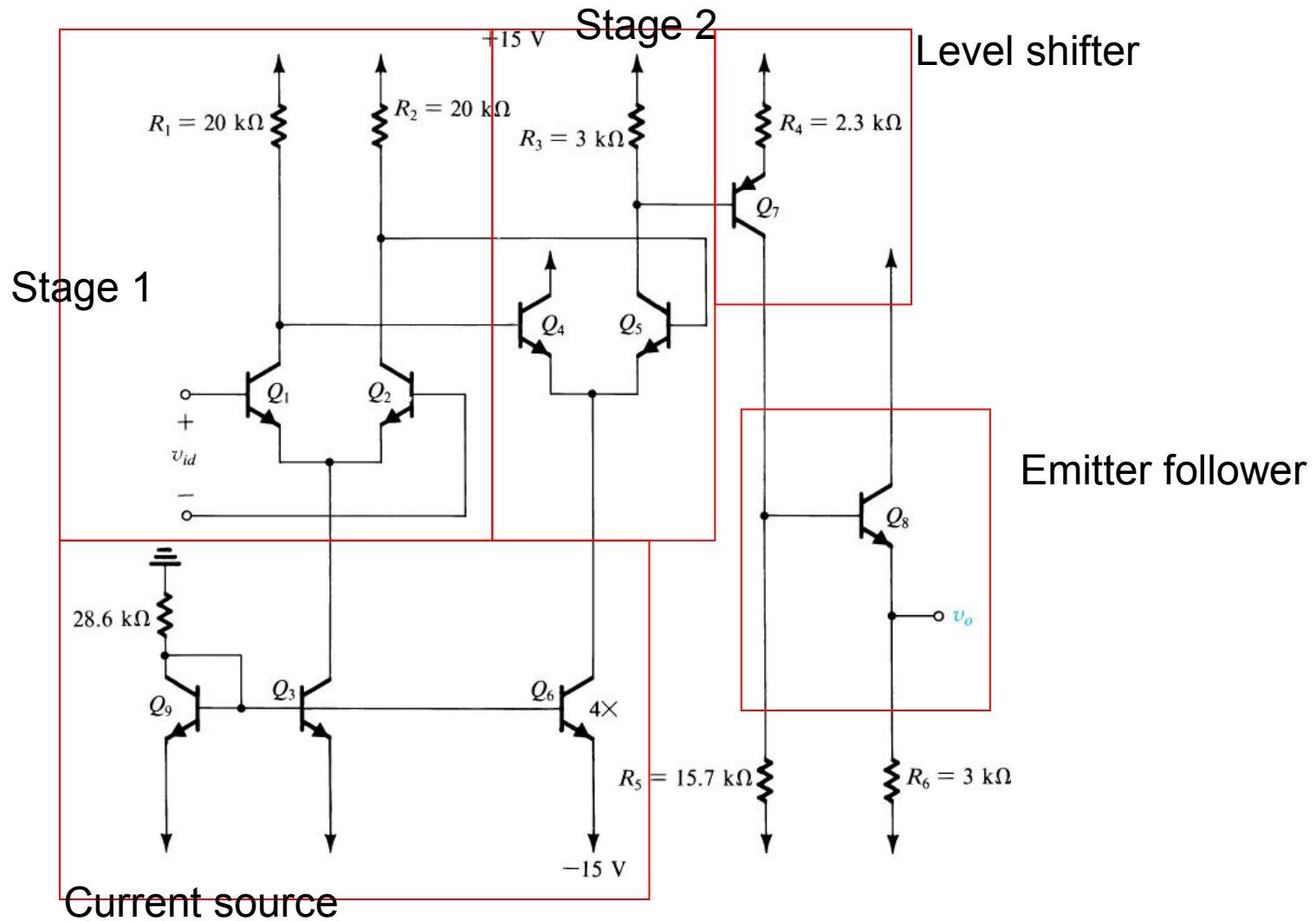
를 만족해야 함.

$$A_1 = -g_{m1} (r_{o2} \parallel r_{o4})$$

$$A_2 = -g_{m6} (r_{o6} \parallel r_{o7})$$

If not, offset voltage at one of the input nodes is inevitable.

A bipolar Op Amp.



DC bias currents & voltages

